Amendments to the Claims:

1. (Currently Amended) A semiconductor package, comprising:

a semiconductor chip having an upper surface provided with a plurality of input/output pads thereon;

a chip paddle adjacent a bottom surface of the semiconductor chip, ~~said~~ **the** chip paddle having an upper surface and a lower surface;

a plurality of leads surrounding the chip paddle and having upper and lower surfaces, wherein the chip paddle has a maximum thickness which exceeds a maximum thickness of each of the leads **and the upper surfaces of the leads reside on a common plane which extends between the upper and lower surfaces of the chip paddle** ;

conductive wires for electrically connecting the input/output pads of the semiconductor chip to the leads; and

a package body comprised of an encapsulation material that encapsulates the semiconductor chip, the conductive wires, the chip paddle and the leads, wherein **at least** portions of the **lower surfaces of the** chip paddle and the leads are externally exposed ~~at a bottom surface of the chip paddle and the leads~~ in **a common exterior surface of** the package body.

2. (Cancelled)

3. (Cancelled)

4. (Previously Presented) The semiconductor package as set forth in claim 1, wherein:

the lower surface of the chip paddle and the lower surface of each of the leads are in a common plane.

5. (Previously Presented) The semiconductor package as set forth in claim 1, wherein:

the chip paddle is bonded to a bottom surface of the semiconductor chip with an adhesive.

6. (Previously Presented) The semiconductor package as set forth in claim 1, wherein:

each of the leads has an etched part at an end facing the chip paddle.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) A packaged semiconductor, comprising:

a chip paddle adapted to receive a semiconductor chip, said chip paddle having an upper surface, a lower surface, and an intermediate surface positioned between and parallel to the upper surface and the lower surface**, the lower and intermediate surfaces collectively defining a lower side area of the chip paddle, the intermediate surface being about 10% to about 90% of the lower side area**;

a plurality of leads surrounding the chip paddle, the chip paddle and the leads comprising a leadframe wherein the intermediate surface of the chip paddle and at least one portion of an upper surface of each of the leads are in approximately a common plane, and wherein the chip paddle has a maximum thickness which exceeds a maximum thickness of each of the leads; and

the leadframe being adapted to receive a package body comprised of encapsulation material for encapsulating the chip paddle and the leads, wherein portions of the chip paddle and the leads are externally exposed in the package body **and the intermediate surface of the chip paddle is located inside the package body**.

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Previously Presented) The packaged semiconductor as set forth in claim 13, wherein:

each of the leads has an etched part at an end facing the chip paddle.

18. (Previously Presented) The packaged semiconductor as set forth in claim 13, wherein:

each of the leads has a lower surface which is externally exposed in the package body.

19. (Currently Amended) A package for mounting a semiconductor chip, comprising:

a leadframe, comprising:

a chip paddle **defining a lower side area and an etched portion in the lower side area**, wherein **the etched portion is about 10% to about 90% of the lower side area and** a surface of the chip paddle is externally exposed in the package; and

a plurality of leads surrounding the chip paddle, wherein a surface of each of the plurality of leads is externally exposed in the package;

means for receiving encapsulating material for encapsulating the leadframe;

means for locking the encapsulating means to the chip paddle;

means for providing a fluid path for the encapsulating means during encapsulation of the leadframe; and

said means for locking and said means for providing a fluid path being formed from a void caused by said chip paddle being of a maximum thickness which exceeds a maximum thickness of each of the leads.

20. (Cancelled)

21. (Cancelled)

22. (Currently Amended) The package as set forth in claim ~~21~~ **19**, wherein the means for locking comprises the etched portion.

23. (Currently Amended) The package as set forth in claim ~~21~~ **19**, wherein the means for providing a fluid path comprises the etched portion.

24. (Cancelled)

25. (Currently Amended) The package as set forth in claim ~~21~~ **19**, wherein the etched portion is located inside the package body, a lower surface of the chip paddle and a lower surface of each of the plurality of leads are in approximately a common plane, the chip paddle is bonded to a bottom surface of a semiconductor chip and at least one of the plurality of leads has an etched part at an end facing the chip paddle.